

**FLEXIBLE DIELECTRIC ELECTRONIC SUBSTRATE  
AND METHOD FOR MAKING SAME**

5       **[ 001]**       This Application is a continuation of U.S. Patent Application Serial Number 09/578,583 filed May 25, 2000, which is a continuation-in-part of U.S. Patent Application Serial Number 09/412,052 filed October 4, 1999 (now U.S. Patent 6,288,905) and of U.S. Patent application Serial Number 09/524,148 filed March 14, 2000 (now U.S. Patent 6,376,769), and claims the benefit of U.S. Provisional Application Serial Number 60/136,917 filed June 1, 1999, of U.S. Provisional Application Serial Number 60/141,344 filed June 28, 1999, of U.S. Provisional Application Serial Number 60/150,437 filed August 24, 1999, of U.S. Provisional Application Serial Number 60/150,869 filed August 26, 1999, of U.S. Provisional Application Serial Number 60/180,544 filed February 7, 2000, and of U.S. Provisional Application Serial Number 60/180,907 filed February 8, 2000.

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**[ 002]**       The present invention relates to a flexible electronic substrate and, in particular, to a molecularly flexible electronic substrate including a molecularly flexible dielectric adhesive having a low modulus of elasticity.

20       **[ 003]**       As semiconductor integrated circuit technology has advanced to greatly increase the amount and operating speed of the circuitry that can be fabricated on a single semiconductor chip, it has become more difficult to effectively utilize such integrated circuits due to the greatly increased number of input and output connections to the chip and the decreasing spacing or pitch of those connections. The connection problem has become more severe where the numbers of connections exceeds that conveniently or economically attainable in a conventional mechanical package.

25       **[ 004]**       One approach to solve this problem utilizes semiconductor chips mounted with contacts against and connecting to corresponding contacts on the next-level circuit board, the so-called "flip-chip" mounting, in which the contacts on the next-level circuit board are of substantially the same size and of the same pitch as are those on the semiconductor chip. Problems arise because the pitch of the semiconductor chip connections is much finer than the pitch attainable on

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conventional mechanical packages and printed wiring circuit boards to which such semiconductor chips are mounted. In addition, differences in thermal expansion between the semiconductor chip and the next-level circuit board produce thermally-induced stress that leads to failure or degradation of the interconnections when  
5 exposed to thermal cycling, which stress is often exacerbated by the rigidity of solder interconnections therebetween.

[ 005] One solution to these problems employs an intermediate substrate between the semiconductor chip and the next-level circuit board to absorb some of the thermally-induced stress, and also to allow the fanning out of the connections to the  
10 semiconductor chip to permit a larger contact size and pitch that is compatible with conventional printed wiring circuit board technology. If the intermediate substrate is substantially larger than the size of the semiconductor chip, then the advantage of small chip size is lost, as is the advantage of short electrical lead length that improves the ability to operate the circuit at very high operating frequencies. While this has  
15 been addressed by reducing the size of the intermediate substrate and employing next-level substrate technologies capable of finer line widths and smaller features, the rigidity of the intermediate substrate has again posed some difficulties. Electronic packages where the perimeter of the intermediate substrate is no more than about 20% larger than the perimeter of the semiconductor chip mounted thereon are often  
20 referred to as "chip scale packages," although larger packages are often also referred to as "chip scale packages."

[ 006] The difficulties of rigid intermediate substrates has been addressed by making the substrates of specialized materials that are referred to as being "flexible," such as thin polyimide and other so-called "flexible" conventional substrates on which  
25 printed wiring conductors and plated through holes can be formed by conventional methods. But, such substrate materials are not truly flexible in that they do not have a low modulus of elasticity, but only flex to a greater extent because they have been made of thinner material having a high modulus of elasticity. Conventional materials, such as polyimide sheet, have a high modulus of elasticity, e.g., a modulus greater  
30 than 70,000 kg/cm<sup>2</sup> (1,000,000 psi). In addition, the use of such materials and conventional fabrication methods results in an increased cost that is undesirable and

may require assembly processes that are more difficult or expensive to perform.

[ 007] In addition, enclosed cavity packages are often preferred due to their resistance to the entry of moisture, such as the hermetically-sealed packages usually employed in high reliability, military, aerospace, and medical electronic applications, and in applications of optical devices and frequency-sensitive communication devices. Such packages are generally metal or ceramic with seals formed of glass or metal solders or brazing. The ability of a package to resist the entry of moisture, or to allow the easy exit of moisture, is of importance to reliability of operation. Typically, hermetic type packages are most reliable; lidded packages are less reliable than hermetic packages, but are more reliable than are glob-top, molded or encapsulated packages.

[ 008] Conventional hermetic cavity type packages are very expensive, due to the metal and/or ceramic package, the slow methods utilized for sealing the rim of the package lid and high labor content. Lidded cavity packages are much less expensive than hermetic packages, but are still expensive as compared to encapsulated packages, such as the molded epoxy or molded plastic encapsulated packages, that are employed in about 95-99% of commercial electronic applications. Even glob-top encapsulated packaging is more expensive than molded packages due to the inherently slow process of dispensing precise amounts of encapsulant, even using precision dispensing equipment. In addition, conductive adhesive connections are unfamiliar to an industry that has long utilized and relied upon solder connections.

[ 009] Accordingly, there is a need for an electronic substrate or interposer that is suitable for a solder connection, and that avoids some of the technical disadvantage of conventional molded packages without the high cost of conventional hermetic packages. In addition, it would be desirable that such substrate or interposer be suitable for high-density (e.g., chip-scale) packages.

[ 010] To this end, the flexible dielectric electronic substrate of the present invention comprises a layer of flexible dielectric adhesive having a modulus of elasticity less than about 500,000 psi, having a glass transition temperature less than about 0°C, having the ability to withstand soldering at about 220°C; and a metal foil on one surface of the layer of flexible dielectric adhesive, wherein the metal foil is

patterned to define a pattern of electrical conductors having a plurality of contact sites for receiving the contacts of an electronic device.

[ 011] Further, a method for making a flexible electronic substrate for receiving an electronic device comprises:

- 5                   providing a sheet of metal foil;
- providing at least one layer of a flexible dielectric adhesive having a modulus of elasticity less than about 500,000 psi on one surface of the sheet of metal foil, the layer of flexible dielectric adhesive having a plurality of via openings therein;
- 10                  building up conductive material on the metal foil to fill the via openings, thereby forming conductive vias therein;
- patterning the metal foil to form a pattern of contacts and conductors electrically connected to the conductive vias in the flexible dielectric adhesive layer; and
- 15                  plating at least one of the conductive vias and the contacts of the patterned metal foil to provide external contacts.

#### BRIEF DESCRIPTION OF THE DRAWING

20   [ 012]        The detailed description of the preferred embodiments of the present arrangement will be more easily and better understood when read in conjunction with the FIGURES of the Drawing which include:

                  [ 013]        FIGURES 1 and 2 are side cross-sectional schematic diagrams of alternative example embodiments of an electronic package including a substrate  
25                   according to the present arrangement attached to a next-level substrate;

                  [ 014]        FIGURES 3A and 3B are schematic diagrams of example “fan-out” contact patterns useful with an interposer in the embodiments of FIGURES 1-2;

                  [ 015]        FIGURE 4 is a side cross-sectional schematic diagram showing additional detail of the example embodiment of an electronic package according to the  
30                   present arrangement as shown in FIGURE 1;

                  [ 016]        FIGURES 5 and 6 are schematic diagrams of example fan-out contact

patterns useful with an interposer in the embodiment of FIGURE 4, as well as those of FIGURES 1-2;

[ 017] FIGURES 7A, 7B and 7C are side cross-sectional schematic diagrams illustrating the fabrication of an interposer of the sort described in relation to  
5 FIGURES 1 - 6, and FIGURE 7D shows the interposer so made attached to a semiconductor wafer;

[ 018] FIGURES 8A and 8B are plan and cross-sectional schematic diagrams, respectively, of an interposer in accordance with the present arrangement and employing plural layers of dielectric material;

10 [ 019] FIGURE 9 is a side cross-sectional schematic diagram of an alternative embodiment of a flexible interposer according to the present arrangement;

[ 020] FIGURES 10, 11 and 12 are side cross-sectional schematic diagrams illustrating stages in the fabrication and application of another alternate embodiment of a flexible interposer 110 according to the present arrangement; and

15 [ 021] FIGURES 11A and 11B are side cross-sectional schematic diagrams illustrating fabrication additional to the stage of FIGURE 11 for producing another alternate embodiment according to the present arrangement.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

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[ 022] A typical conventional electronic package includes a semiconductor chip or die attached to an intermediate laminated substrate, such as an FR4 laminate, by a die attach adhesive. Bond wires, which are fine gold or aluminum wires, connect the contacts of a semiconductor chip to corresponding conductors on a substrate  
25 which are in turn connected to conductors on a next-level substrate by connections which may be of solder or electrically-conductive adhesive. The semiconductor chip and bond wires may be protected by a lid or cover, or by a moisture-resistant coating or an encapsulant. Alternatively, the semiconductor chip may be mounted to the substrate in a conventional "flip-chip" manner.

30 [ 023] Mechanical stresses arise due to the differences in the coefficients of thermal expansion (CTE) of the different materials utilized in such conventional

module and the high moduli of elasticity (ME), i.e. rigidity, thereof. A silicon semiconductor die has a CTE of about 3 ppm/°C, an adhesive has a CTE of about 40 ppm/°C, the substrate has a CTE of about 17 ppm/°C, and an encapsulant has a CTE of about 30 ppm/°C. A silicon semiconductor die has a ME of about 700,000-1,400,000 kg/cm<sup>2</sup> (about 10,000,000-20,000,000 psi), the adhesive has a ME of about 70,000 kg/cm<sup>2</sup> (about 1,000,000 psi), and the substrate and encapsulant have a ME of about 140,000 kg/cm<sup>2</sup> (about 2,000,000 psi). Principally, stress arises in the adhesive and at the interfaces of the adhesive with the chip and the substrate, and to a lesser extent in the encapsulant. The magnitude of the stress depends upon the magnitude of the differences in CTE, the curing temperature of the adhesive and the encapsulant, and the modulus of elasticity of the adhesive and encapsulant.

[ 024] On the other hand, by employing an intrinsically or molecularly flexible “interposer” or intermediate substrate, the stress build up of the prior art packages is avoided and reliable electronic packages, including chip-scale packages, may be inexpensively made. An intrinsically flexible or molecularly flexible material is a material that is flexible as a result of its molecular structure, and not just because it has been formed into a very thin sheet. Steel, aluminum and glass can be flexed if made thin enough, but none is intrinsically flexible. As used herein, flexible means a material that has a modulus of elasticity that is less than about 35,000 kg/cm<sup>2</sup> (500,000 psi) and that withstands an elongation of at least 30% in length without failure. Thus, conventional substrate materials, such as FR4 laminate which has a modulus of elasticity of about 140,000 kg/cm<sup>2</sup> (about 2,000,000 psi) and polyimide which has a modulus of elasticity of about 140,000 kg/cm<sup>2</sup> (about 2,000,000 psi), and bismaleimide-triazine, are not flexible as that term is used herein.

[ 025] FIGURE 1 is a side cross-sectional schematic diagram of an example embodiment of an electronic package 100 having a substrate 110 according to the present arrangement attached to a next-level substrate 140. Package 100 includes a flexible interposer 110 which is a substrate upon which an electronic device, for example, semiconductor chip 120, is attached. Contacts on the bottom face of chip 120 are directly connected to contacts 112 of interposer 110 by interconnections 124, which may be of solder or an electrically-conductive flexible adhesive. Where

support for chip 120 in addition to that provided by connections 124 is desired, flexible dielectric underfill adhesive 126 is employed to fill the volume between chip 120 and interposer 110 that is not filled by flexible connections 124. Solderable contacts 114 on interposer 110 correspond to contacts 112 on the opposing surface thereof, and provide contacts for connections 134 between package 100 and conductors on next-level circuit substrate 140. Connections 134 may be conventional solder connections or electrically-conductive adhesive as in a ball grid array (BGA) package, and an underfill material is not required between package 100 and next-level substrate 140.

[ 026] Preferably, flexible adhesive interposer 110 comprises a layer of flexible dielectric adhesive on a sheet of metal foil, such as a copper, copper alloy, nickel, aluminum or other electrically-conductive metal or an alloy thereof, that is subsequently etched to define the pattern of contacts 114. Via holes in the flexible dielectric layer are filled with flexible electrically conductive adhesive to provide electrical connection to contacts 112. The flexible adhesives of interposer 110 have a modulus of elasticity that is less than about 35,000 kg/cm<sup>2</sup> (about 500,000 psi), and preferably is less than about 14,000 kg/cm<sup>2</sup> (about 200,000 psi), and more preferably is about about 7,000 kg/cm<sup>2</sup> (about 100,000 psi), and most preferably is about 1,400 kg/cm<sup>2</sup> (about 20,000 psi). In addition, such flexible adhesives are able to withstand the high temperature to which they will be subjected by soldering operations, e.g., the 220°C melting temperature of solder. Preferably, the flexible adhesive can withstand a temperature of up to 300°C for 1-2 minutes without change of shape, dimension or mechanical strength.

[ 027] Suitable flexible dielectric adhesives include, for example, types CC7450, ESP7450, ESP7550, ESP7670 and ESP7675 screen-printable flexible thermosetting dielectric adhesives and type UVS7450 photo-etchable flexible thermosetting dielectric adhesive, all of which have a modulus of elasticity of about 1,400 kg/cm<sup>2</sup> (about 20,000 psi) and a CTE of about 100 ppm/°C, and are available from AI Technology, Inc., located in Princeton, New Jersey. Suitable flexible electrically-conductive adhesives that may be employed to fill via holes in the dielectric layer of interposer 110 or to form connections 124 include types ESP8350,

ESP8450, ESS8450, ESS8459, and ESP8550 flexible electrically-conductive thermosetting adhesive also available from AI Technology, Inc. Flexible interposer 110 and the making thereof is described in detail herein below.

[ 028] It is noted that, because flexible adhesive interposer 110 is molecularly flexible, and because flexible conductors 112 thereof are solderable, interconnections 124 and/or 134 may preferably be metal solder connections such as are known and in widespread use in the flip chip mounting of electrical devices.

[ 029] Lid or cover 130 is attached to interposer 110 by an adhesive to enclose chip 120 and provide mechanical protection therefor. Where additional mechanical support is desired, a flexible adhesive pad 132 may be employed to join the inner surface of lid 130 to the upper face of chip 120. Lid 130 may be plastic, glass, ceramic or metal, as desired. Where it is desired to remove heat from chip 120, lid 130 may be made of a thermally conductive material, such as copper, brass, steel or aluminum, and flexible adhesive 132 may include thermally-conductive particles to provide a thermal connection between chip 120 and lid 130 from whence heat may be dissipated. Where it is desired that light be permitted to pass through lid 130 and impinge upon chip 120, lid 130 or at least the top thereof may be optically transparent to light of the desired wavelength(s). In addition, an optional metallic rim 118 may be provided on flexible adhesive interposer 110 to stiffen interposer 110 in the peripheral region thereof where lid 130 is attached.

[ 030] It is also noted that the flexible adhesive bumps and the solder bumps of package 100 that form respective connections 124 may be deposited onto or otherwise applied to chip 120, either at the semiconductor die level or at the semiconductor wafer level, before chip 120 is attached to flexible adhesive interposer 110, or may be applied to contacts 112 of interposer 110.

[ 031] FIGURE 2 is a side cross-sectional schematic diagram of an alternative example embodiment of an electronic package 100" according to the present arrangement attached to a next-level substrate 140. Package 100", like package 100, includes flexible interposer 110, and electronic device or chip 120 attached thereto, but with contacts on chip 120 connected to contacts 112' of interposer 110 by bond wires 125. Bond wires 124 are preferably fine gold or aluminum wires, such as are



known and in widespread use in electrical devices. Contacts 112 may be formed of standard lead-frame metals, such as copper, nickel or kovar alloy, which and may also form a die-attach pedestal under chip 120 as well. Chip 120 is attached to flexible adhesive interposer 110 by a flexible or a rigid die-attach adhesive 126'. Interposer contacts 114 provide contacts for BGA solder or conductive adhesive connections 134 between package 100" and conductors on next-level circuit substrate 140; without underfill. Lid 130 attached to interposer 110 provides mechanical protection for chip 120. An optional flexible adhesive pad 132 may be employed to provide added mechanical support and covering for chip 120, and optional metallic rim 118 may be provided for stiffening, all as described above.

[ 032] It is noted that because flexible adhesive interposer 110 of packages 100, 100" of FIGURES 1-2 is molecularly flexible as defined above, one or both of connections 124 and connections 134 may be metal solder connections such as the so-called "C<sup>4</sup>" solder connections known and in widespread use in the flip chip mounting of electrical devices, without thermally-induced stresses jeopardizing the integrity and reliability of the electrical connections they provide, despite the very rigid nature of the solder, e.g., a modulus of elasticity of about of about 700,000 kg/cm<sup>2</sup> (about 10,000,000 psi) and a CTE of about 20-25 ppm/°C.

[ 033] Where the flexible interposer 110 of the packages 100, 100" of FIGURES 1-2 allows moisture to enter into the volume of cavity 136 defined by lid 130, chip 120 and flexible interposer 110, moisture will also exit cavity 136 with relative ease, however, if moisture is present within cavity 136 and the temperature were to drop, then moisture may condense on the surfaces of interposer 110, chip 120 and lid 130 within cavity 136. The presence of such condensed moisture could lead to corrosion or oxidation of certain materials such as the metals of which various conductors and contacts are formed. Such condensation is most likely to occur while chip 120 is not being operated, e.g, while it is unpowered. When chip 120 is powered, it is likely that the heat generated thereby will raise the temperature of chip 120 and so avoid condensation on chip 120. Thus, condensation is likely to be only intermittent at worst and to occur during an unpowered condition.

[ 034] Where semiconductor chip 120 is attached to flexible adhesive

interposer 110 in a flip-chip arrangement as in FIGURE 1, for example, dielectric adhesive underfill 126 protects the contacts of chip 120 and flexible adhesive interposer 110 against condensation. In addition, where moisture is expected to enter cavity 136, it is preferred that the dielectric adhesive of underfill 126 be hydrophobic to further diminish the possibility of condensation forming on the contacts of chip 120 and flexible adhesive interposer 110. Similarly, where semiconductor chip 120 is mounted for wire-bond connections as in FIGURE 2, the contacts of chip 120 are exposed and chip 120 may be covered with a suitable protective coating 128, preferably a flexible hydrophobic coating, to reduce the possibility of corrosion. Suitable hydrophobic adhesives for such underfill and coating include types CP7135, CP7130 and ESP7450 flexible hydrophobic dielectric adhesives available from AI Technology, Inc., in which the carrier medium is typically a non-polar hydrophobic polymer.

[ 035] It is also noted that where lid 130 includes a pre-applied adhesive around the edges thereof that adhesively attach to flexible adhesive interposer 110, packages 100, 100" may be assembled in an in-line process, such as by standard pick-and-place component mounting equipment. While such lids 130 may be provided in several ways including by dispensing adhesive onto each lid or cover, or by applying an adhesive preform to each lid or cover, adhesive preform lids and covers as described in U.S. Patent No. 6,136,128 (U.S. Patent Application Serial Number 09/232,936 filed January 19, 1999) entitled "Method Of Making An Adhesive Preform Lid, As For An Electronic Device" and laminated adhesive lids and covers as described in U.S. Patent No. 6,409,859 (U.S. Patent Application Serial Number 09/337,453 filed June 21, 1999) entitled "Method Of Making A Laminated Adhesive Lid, As For An Electronic Device" which are expressly incorporated herein by reference in their entirety, are well suited to packages 100, and 100". With such low cost lids and covers and in-line processing, the cost of packages according to the present arrangement could be comparable to the cost of glob-top and molded encapsulation packages.

[ 036] FIGURES 3A and 3B are schematic diagrammatic illustrations of example "fan-out" patterns useful with a flexible adhesive interposer 110 (shown in

part) of the embodiments of FIGURES 1-2. Semiconductor chip 120 is fabricated by conventional methods that permit very fine features to be formed therein, e.g., dimensions of about 1  $\mu\text{m}$  and larger, including very small size electrical conductors and contacts that are also very closely spaced. But such features are too fine to be compatible with typical low-cost conventional next-level substrates 140, such as FR4 printed wiring circuit boards, which typically have features of at least 50  $\mu\text{m}$  (about 2 mils) and larger. Because the pattern of contacts 112 of flexible adhesive interposer 110 that correspond to the pattern of contacts of semiconductor chip 120 need not be the same pattern as the pattern of contacts 114 of flexible adhesive interposer 110 that correspond to a pattern of contacts on next-level substrate 140, a fan-out arrangement of contacts 112, 114 and conductors 113 may be employed to space apart contacts 112 and 114 that complete connections between contacts on semiconductor chip 120 and those on next-level substrate 140, respectively.

[ 037] In FIGURE 3A, for example, contacts 112a - 112f to which contacts of semiconductor chip 120 attach may be 50 $\mu\text{m}$  (about 2 mils) in diameter and at a pitch (center-to-center spacing) of 100  $\mu\text{m}$  (about 4 mils), and are on a first surface of flexible adhesive layer 111 of interposer 110, which layer 111 is shown partially removed. Contacts 114a - 114f to which contacts of next-level substrate 140 attach may be 100 $\mu\text{m}$  (about 4 mils) in diameter and at a pitch (center-to-center spacing) of 300  $\mu\text{m}$  (about 12 mils), and are on a second and opposing surface of flexible adhesive layer 111 of interposer 110. Conductors 113 connect corresponding ones of contacts 112 and 114, e.g., connect contacts 112a and 114a, connect 112b and 114b, and so forth, and may be quite fine, e.g., about 25-50  $\mu\text{m}$  wide, and of varying length to further space contacts 114 apart. Conductors 113 are in a sequence of lengths to remove contact 114a from contact 112a by about 0.5 mm (about 20 mils), contact 114b from contact 112b by about 1 mm (about 40 mils) and contact 114c from contact 112c by about 1.5 mm (about 60 mils). Flexible conductive adhesive vias 115 through flexible adhesive layer 111 can be much smaller than contacts 114, e.g., about 50  $\mu\text{m}$  (about 2 mils) in diameter.

[ 038] Although conductors 113 are shown in FIGURE 3A as being on the far surface of flexible adhesive layer 111 and connecting to contacts 114 through flexible

conductive adhesive vias 115, conductors 113 could be on the near surface of flexible adhesive layer 111 and connect to contacts 112 through conductive vias thereat.

Flexible adhesive layer 111 is resistant to the solvents and other chemicals used in forming conductors 113, contacts 114 and flexible conductive adhesive vias 115

thereon. In addition, it is noted that the locations of contacts 114 on interposer 110 may be outside the periphery of semiconductor chip 120, as illustrated, may be within the periphery of chip 120, or may be both outside and within the periphery of chip 120, i.e. at any location on flexible adhesive interposer 114.

[ 039] In FIGURE 3B, for example, an alternative fan-out arrangement not only expands the size and spacing of contacts 114 with respect to contacts 112 as in FIGURE 3A, but also provides for contacts 112 and 114 to be in mirror image patterns, as is particularly useful where a semiconductor chip that was mounted in the manner of FIGURE 2 is to be utilized in a package of the sort of FIGURE 1 in which it is to be mounted in a flip-chip manner which reverses the pattern of its contacts, for example, as viewed from the direction of next-level substrate 140. This reversal is removed by the pattern of conductors 113 which connect contacts 112 on the leftward edge of semiconductor chip 120 (shown in phantom) with the corresponding contacts 114 on the rightward portion of interposer 110, and also connect contacts 112 on the rightward edge of semiconductor chip 120 with the corresponding contacts 114 on the leftward portion of interposer 110. In the example of FIGURE 3B, contacts 114 are large and rectangular, as might be useful where contacts 114 are to come into electrical contact with external conductors, as in a contact-type card or tag as could be employed for ingress/egress access, identification of personnel or equipment or other objects, credit, debit and telephone cards, and the like.

[ 040] Among the additional advantages of the foregoing packages 100, 100" are that they employ materials that are readily available at reasonable cost and may be fabricated utilizing standard "pick-and-place" equipment to attach semiconductor chips 120 and lids 130, for example, on an inherently fast, assembly-line arrangement, and so inherently offer the advantage of low cost, e.g., no more than two times the cost of the lowest cost conventional molded electronic packages.

[ 041] Alternatively, cavity 136 of packages 100, 100" may be substantially

filled with encapsulant 137. In these cases, lid or cover 130 may be utilized as an encapsulating form or mold and then may remain or be removed, or cover 130 may be eliminated and an encapsulating mold used. It is noted that the equipment and other infrastructure for molding encapsulant around electronic devices is known and available and so is easily utilized in relation to the present arrangement at low cost. Molding may be performed for “strips” and continuous reels having a series of electronic devices in a line thereon (one-dimensional arrays) or “panels” or wide continuous reels having a fixed number of electronic devices across the width thereof (two-dimensional arrays), similar to molding of conventional lead-frame packages. Depositing and finishing of solder balls 134 may likewise be performed on such one- and two-dimensional arrays of devices. The strips, continuous reel, panel or other arrangement may employ alignment holes therein for proper positioning of the various features of packages 100, 100' and 100''. Further, the resistance of the molded package to the entry of moisture is likewise known, and may be improved by the fact that moisture may escape through the flexible adhesive of interposer 110, which would reduce the effect of expansion of trapped moisture due to heating during soldering of surface mount technology (SMT) packages, sometimes referred to as the “pop-corn” effect. Where semiconductor chip 120 is mounted in a flip-chip manner, an electrically-conductive hydrophobic flexible is preferred for connections between chip 120 and interposer 110 so as to further resist moisture, and a hydrophobic adhesive underfill 126 is likewise preferably a hydrophobic adhesive.

[ 042]        Suitable materials for encapsulant 137 include standard rigid encapsulants, such as known epoxy and liquid epoxy compounds utilized for molded and glob-top encapsulation, that have a CTE of about 30 ppm/°C or less and a high modulus of elasticity, e.g., about 140,000 kg/cm<sup>2</sup> (about 2,000,000 psi), and flexible adhesive encapsulants, such as the flexible dielectric adhesives identified above.

[ 043]        FIGURE 4 is a side cross-sectional schematic diagram showing additional detail of the example embodiment of an electronic package similar to package 100 of FIGURE 1. Electronic device (chip or die) 120 is mounted to flexible adhesive interposer 110 in a flip-chip manner by connections 124, which may be solder connections or flexible electrically-conductive adhesive, and optional flexible

dielectric underfill adhesive 126. Flexible adhesive interposer 110 comprises flexible adhesive layer 111 and a metal layer providing conductors 113 thereon. Flexible adhesive layer 111 has via holes therethrough in which are conductive vias 112 which are a flexible electrically-conductive adhesive of like flexibility (i.e. modulus of elasticity) to that of flexible dielectric adhesive layer 111. The metal layer is patterned, such as by photo etching or printing, to provide conductors 113 between conductive vias 112 and metal contacts 114 on which are formed solder ball or solder bump contacts 134.

[ 044] In an example form of package 100 of FIGURE 4, chip 120 may be about 25-500  $\mu\text{m}$  (about 1-20 mils) thick, and more typically about 250-500  $\mu\text{m}$  (about 10-20 mils) thick, and flexible adhesive layer 111 is about 75-250  $\mu\text{m}$  (about 3-10 mils) thick with about 50-250  $\mu\text{m}$  (about 2-10 mils) thick copper conductors 113 and contacts 114 thereon. Suitable flexible dielectric adhesives for interposer 110 include types CC7450, ESP7450, ESP7550, ESP7670 and ESP7675 flexible thermosetting adhesives and type UVS7450 flexible thermosetting adhesive, which is suitable for use with conventional UV photoresist and photo-etching chemicals and solvents, each of which is a polymer adhesive available from AI Technology, Inc. located in Princeton, New Jersey, or other suitable flexible adhesive, and each of which has suitable properties, such as low dielectric constant, low dielectric loss, good temperature stability, low sensitivity to moisture and the like. Conductive vias 112 of flexible electrically conductive adhesive are about 50-100  $\mu\text{m}$  (about 2-4 mils) in diameter, as are conductive connections 124. Suitable electrically-conductive adhesives for connections 124 include type PSS8150 SOLDER-SUB<sup>®</sup> flexible thermoplastic adhesive or type ESS8450 SOLDER-SUB<sup>®</sup> adhesive, as well as types ESP8350, ESP8450, ESS8459, and ESP8550, each of which is a thermosetting electrically-conductive polymer adhesive also available from AI Technology, Inc., or other suitable flexible conductive adhesive, which desirably reduces the thermally-induced stress due to the temperature of the package, both in processing, such as in soldering solder connections 134, and in operation whether due to environment and power dissipation of chip 120. Suitable underfill adhesive 126 includes type MEE7650-5 flexible dielectric polymer adhesive, as well as types CP7135, CP7130

and ESP7450 flexible dielectric adhesives, all also available from AI Technology. Solder bumps 124 and/or 134 are about 125-250  $\mu\text{m}$  (about 5-10 mils) in diameter and somewhat less in height after being reflowed. Lid 130 is typically about 0.5 - 0.75 mm (about 20-30 mils) thick and may be attached to flexible adhesive interposer 110 with the same adhesive as is employed for adhesive underfill 126, for example. Optional adhesive interface 132 may be a dielectric adhesive such as type ESP7450 or type ESP7670 where additional mechanical support is desired, or may be an electrically conductive adhesive such as type PSS8150 SOLDER-SUB<sup>®</sup> adhesive or type ESS8450 SOLDER-SUB<sup>®</sup> adhesive where an electrical connection between chip 120 and cover 130 is also desired, or may be a thermally-conductive adhesive such as types ESP7455 and ESP7675 thermally conductive dielectric thermosetting adhesives also available from AI Technology. Lid 130 may be plastic or metal, and preferably is metal where either electrical conduction or thermal conduction through lid 130 is desired, unless an electrically-conductive or thermally-conductive plastic is suitable.

[ 045] It is noted that flexible adhesive interposer 110 is well suited for fan out between the contacts of chip 120 and those of a next-level substrate 140, as illustrated in FIGURE 4 by the spacing of the contacts of semiconductor chip 120 and thus of ones of connections 124 and conductive vias 112 being closer than is the spacing of ones of contacts 114 and solder bumps 134, as in a ball-grid-array (BGA) device. FIGURE 5 is a schematic diagram of an example fan-out contact pattern useful with a flexible adhesive interposer 110 in the embodiment of FIGURE 4, as well as in the embodiments of FIGURES 1-2, and may accommodate standard, conventional or non-standard contact patterns. For example, FIGURE 5 illustrates a chip 120 (shown in phantom) having its contacts located around the periphery thereof attaching to conductive vias 112, e.g., 112a, 112b, and so forth, which are connected by conductors 113 to corresponding contacts 114, e.g., 114a, 114b, and so forth, respectively, located on two concentric rectangular patterns or arrays R1 and R2 of contacts. Conductive vias 112 may be about 75 $\mu\text{m}$  (about 3 mils) in diameter and at a 150  $\mu\text{m}$  (about 6-mil) pitch and connect to corresponding contacts 114 through 75  $\mu\text{m}$  (about 3-mil) wide conductors 113. Contacts 114 may be about 125-250  $\mu\text{m}$  (about 5-10 mils) in diameter and at a 1 mm (about 40-mil) pitch with respect to conductors

113 if on pattern R1 and at a 2 mm (about 80-mil) or greater pitch if on pattern R2.

[ 046]           Similarly, FIGURE 6 illustrates a semiconductor chip 120 (shown in phantom) having contacts located in a two dimensional or “area array” of positions, which may be a regular or an arbitrary or irregular array of positions, at which are  
5       conductive vias 112 that are connected by conductors 113 to an array of contacts 114 located in another two dimensional or area array of positions, which may be a regular array or may be an arbitrary or irregular array of positions. Typical dimensions thereof may be the same as or similar to those above in relation to FIGURE 5. It is noted that the locations of contacts 114 on interposer 110 may be outside the  
10       periphery of semiconductor chip 120, as illustrated, may be within the periphery of chip 120, or may be both outside and within the periphery of chip 120, i.e. at any location on flexible adhesive interposer 114.

[ 047]           In addition to the advantages of electronic packages 100 and 100” employing flexible adhesive interposer or substrate 110 as described above, flexible  
15       adhesive interposer 110 is made by methods that advantageously avoid many of the costly operations associated with the manufacture of conventional printed circuit wiring boards, such as the drilling of through holes in the substrate and the formation of plated-through conductor holes in the substrate material, the separate manufacture of plural different printed circuit wiring boards that must be laminated together to  
20       form a plural-layer printed circuit board, and the like.

[ 048]           Moreover, flexible adhesive interposer 110 is truly flexible because the adhesive employed therein is molecularly flexible, i.e. it has a low modulus of elasticity, and not just because it is thin as is the case with conventional so-called flexible substrate materials. As a result, flexible adhesive interposer 110 may be  
25       formed employing methods that permit very fine contacts and conductors at very close spacing, i.e. fine pitch. Further, flexible conductive adhesive vias 112 therein can withstand soldering temperature and are coated with a solderable material so as to be compatible with conventional solder ball connection processing, in particular, flip-chip processing. In addition, flexible interposers according to the present arrangement  
30       may be formed and/or applied to semiconductor devices at the semiconductor wafer level to remain with the individual devices when the wafer is singulated to produce



plural semiconductor devices, thereby providing an additional saving of time and cost.

[ 049] Typically, the flexible adhesive interposer according to the present arrangement may be made as follows. A thin metal sheet or foil is provided from which contacts on one side of interposer 110 are formed. The metal foil may be  
5 copper or copper alloy (such as beryllium copper), nickel or nickel alloy, aluminum or aluminum alloy, or other suitable electrically-conductive metal, and preferably is an about 12.5-125  $\mu\text{m}$  (about 0.5 - 5 mils) thick copper-based alloy, with a thickness of about 25-50  $\mu\text{m}$  (about 1-2 mils) being typical. The surface of the metal foil may be prepared to improve the adhesion of an adhesive thereto, such as by abrasion or  
10 etching such as chemical or plasma etching or other suitable method. The metal foil should be patternable, such as by etching, and the desired pattern in photoresist or other suitable pattern-defining material may be applied to the metal foil at this stage. Preferably, the metal foil may also be coated with a solderable material or a pattern thereof, such as one of the coatings described below.

15 [ 050] A pattern of bumps of flexible conductive adhesive is deposited onto the metal foil. The pattern of bumps corresponds to the pattern of contacts of the semiconductor device to which they will connect, and may be deposited, for example, in paste form by dispensing, screen printing, stenciling, ink-jet printing or any other suitable method. The flexible conductive adhesive bumps are then dried, B-staged or  
20 cured. Preferred flexible conductive adhesives include types ESP8350, ESP8450, ESP8550, ESS8450, and ESS8459 which are thermosetting flexible conductive adhesives available from AI Technology that can withstand the high temperatures utilized in soldering. Where the semiconductor device is of small size (e.g., less than 5 mm by 5 mm) so that the conductive vias do not need to be flexible, a more rigid  
25 conductive adhesive such as AI Technology type ESP8680 may be utilized. While the foregoing example adhesives are thermosetting adhesives, thermoplastic adhesives that can withstand soldering temperature may also be utilized.

[ 051] A layer of flexible adhesive 111 is deposited on the metal foil, such as by screen printing, stenciling, paste draw down, or other suitable method, typically  
30 having a thickness of about 50 - 250  $\mu\text{m}$  (about 2-10 mils), but preferably a thickness the same as the height of the conductive bumps or slightly less. Adhesive layer 111

has via holes therethrough defined by the screen, stencil or other printing process or other suitable method, in locations corresponding to the locations of the bumps of flexible conductive adhesive previously deposited. Via holes typically have the same diameter as the conductive adhesive bumps, e.g., about 100  $\mu\text{m}$  (about 4 mils) or larger, and are sized so that the flexible dielectric adhesive will touch the conductive adhesive bumps. Relational alignment holes are also preferably formed in the printing screen and/or stencils to provide for alignment of the patterns of flexible adhesive relative to the stencils, screens, masks and other layers typically utilized in later processing operations, such as etching and other masked operations.

[ 052] Alternatively, the layer of flexible adhesive 111 may be deposited on the metal foil prior to the formation of the conductive adhesive bumps thereon, such as by screen printing, stenciling, paste draw down, or by laminating a sheet of dried or B-staged adhesive thereto, or other suitable method, typically having a thickness of about 50 - 250  $\mu\text{m}$  (about 2-10 mils). In this case, adhesive layer 111 has via holes therethrough defined by the screen, stencil or other printing process or formed by laser drilling, mechanical drilling, mechanical punching, die cutting, photo-etching, plasma etching or other suitable method, in locations corresponding to the locations of the contacts of the semiconductor chip 120 to be attached to interposer 110. Mechanical punching, die cutting and screen printing are preferably employed to form via holes having a diameter of about 100  $\mu\text{m}$  (about 4 mils) or larger, and printing, photo-etching, plasma etching and laser drilling are preferably employed to form via holes having a diameter less than about 100  $\mu\text{m}$  (about 4 mils). Such via hole formation by mechanical means is preferably done in sheets or films of dried or B-staged flexible adhesives prior to their being laminated to the metal foil, and relational alignment holes are also preferably formed therein to provide for alignment of the sheet of flexible adhesive relative to the stencils, screens, masks and other layers typically utilized in later processing operations, such as etching and other masked operations. Where the via holes are formed by plasma etching of flexible adhesive layer 111, the metal etch-defining mask may be temporarily attached to, but kept separated from, the flexible adhesive layer 111 by a thin layer of grease or a suitable low temperature adhesive, such as type MB7060 low-melt-flow temperature adhesive available from

AI Technology which releases at a temperature of about 60 °C. The separation provided by the grease or low-temperature adhesive is beneficial to reduce or avoid heating flexible adhesive layer 111 caused by either the plasma etching or by heating the temporary adhesive to remove of the metal etching mask, which heating of flexible adhesive layer 111 could undesirably cause curing or partial curing thereof.

[ 053] Where the adhesive layer 111 is formed first, and after it is dried, B-staged or cures, as appropriate, the via holes therein are filled with flexible conductive adhesive is deposited, for example, in paste form by dispensing, screen printing, stenciling, ink-jet printing or any other suitable method. The flexible conductive adhesive bumps are sized so as to come into contact with the sides of the via holes in dielectric layer 111 and are then dried, B-staged or cured.

[ 054] Preferred flexible adhesives for layer 111 of flexible adhesive interposer include the types identified above which have the characteristics and properties set forth in the table below:

Characteristic or Parameter	Limit Value	ESP7450 Adhesive	UVS7450 Adhesive
Dielectric Constant	<6.0	<4.0	<4.0
Dielectric Loss	<0.1 @ >60 Hz.	<0.05	<0.05
Dielectric Strength	>19,700 V/mm (>500 V/mil)	>29,600 V/mm (>750 V/mil)	>29,600 V/mm (>750 V/mil)
Modulus of Elasticity	<70,000 kg/cm <sup>2</sup> (<500,000 psi)	1,400 kg/cm <sup>2</sup> (20,000 psi)	1,400 kg/cm <sup>2</sup> (20,000 psi)
Elongation Before Failure	>30%	100% @ 25°C	100% @ 25°C
Glass Transition Temperature	<0 °C	< -20 °C	< -20 °C
Adhesion to Copper (ASTM #D1894)	>1.07 dyne/cm (>6.0 lb/in.)	>1.43 dyne/cm (>8.0 lb/in.)	>1.43 dyne/cm (>8.0 lb/in.)
Moisture Absorption	<0.5%	<0.5%	<0.5%

Chemical Resistance (copper-etching solutions)	Pass	Passes, soaking for 8 hours	Pass, soaking for 8 hours
Solvent Resistance (flux cleaning operations)	Pass	Passes, soaking for 8 hours	Pass, soaking for 8 hours
Thermal Stability and Degradation TGA	<10% weight loss @ >300 °C	<10% weight loss @ >400 °C	<10% weight loss @ >400 °C
Coefficient of Thermal Expansion		100 ppm/°C	100 ppm/°C

10 [ 055] Although a dielectric strength of about 19,700 V/mm (about 500 V/mil) is preferred, only about 11,800 V/mm (about 300 V/mil) is necessary for operability. The flexible conductive adhesive typically exhibits similar mechanical properties, but is electrically conductive due to the presence of suitable amounts of conductive particles therein, for example, spheres, flakes or other shapes of silver, 15 gold, palladium, platinum, or other metal or a combination or alloy thereof, in solid form or plated onto a core.

[ 056] After adhesive layer 111 and conductive vias 112 are B-staged and/or cured sufficiently (i.e. partially or fully), they remain attached to the metal foil and are unaffected by (1) the etching chemicals and solvents utilized thereafter, whether acidic 20 or basic, to etch the pattern of conductors 113 and contacts 114 into the metal foil, and to apply, develop and strip the photo-resists utilized to define the patterns to be etched in the metal foil, and (2) the plating of solderable metal onto metal foil 113 and onto flexible conductive adhesive vias 112.

[ 057] It is preferred that the flexible dielectric adhesive of layer 111 and the 25 electrically-conductive flexible adhesive of vias 112 have respective moduli of elasticity that are in the same range. For example, the modulus of elasticity of either one of the adhesives preferably does not exceed three to five times the modulus of elasticity of the other one of the adhesives. Any spillage or excess of conductive adhesive on the surface of dielectric adhesive layer 111 outside of via conductors 112 30 is wiped off. Flexible conductive adhesives such as types PSS8150, ESP8450 and

ESP8550 thermosetting adhesives, all available from AI Technology, do not affect the types ESP7450 and UVS7450 thermosetting dielectric adhesives utilized for dielectric layer 111. It is preferred that the exposed metal of metal layer 113 at the bottoms of the via holes be coated e.g., by plating, with a suitable oxidation-resistant metal, such as gold, nickel-gold, palladium, platinum, nickel-palladium and the like, prior to filing the via holes with conductive adhesive. It is noted that the metal foil layer 113 may be patterned either before or after the forming of the conductive vias 112 where dielectric layer 111 is applied prior thereto.

[ 058]           Patterning of the metal foil layer 113 is by conventional photo-etching processes to create either contacts 114 overlying conductive vias 112, contacts 114 displaced from conductive vias 112 and joined thereto by conductors 113, or both. Because at least an about 2:1 ratio of the width of an etched feature to the thickness of the metal foil is typically desired, thinner metal foils 113 permit finer contacts and conductors to be obtained. For example, about 50  $\mu\text{m}$  (about 2 mil) wide features and pitch may be obtained with a 25 $\mu\text{m}$  (about 1 mil) thick copper foil. A coating 113a may be applied metal foil 113 and conductive vias 112, such as a layer of silver, gold, palladium, platinum, nickel-gold, nickel-palladium, or other precious metal, or other combinations or alloys thereof, such as by plating, to reduce oxidation, metal migration, and/or inter-metallic degradation. Nickel-gold or gold and nickel-palladium plated coating are preferred for conductive vias 112 and contacts 114, with a thickness of about 5  $\mu\text{m}$  nickel covered by a thickness of about 0.1  $\mu\text{m}$  gold or palladium. Alternatively, metal layer 113 may be patterned after interposer 110 is attached to a next-level substrate such as a semiconductor wafer, as described below.

[ 059]           After the patterning of contacts 114 and conductors 113, conductors 113 may optionally be covered by a layer of flexible dielectric adhesive to prevent unintended electrical contact thereto, e.g., such as by solder bridging. The flexible dielectric adhesive may be the same adhesive employed for flexible adhesive layer 111 or may be another type, such as a flexible photo-polymer that can be patterned and partially removed. The pattern of contacts 114 are conveniently not covered where such flexible dielectric adhesive is deposited by screen printing, stenciling or other method allowing for patterned deposition. Although in many cases the patterns

of contacts on electronic device 120 and on next-level substrate 140 are predetermined and so the pattern of conductive vias 112, contacts 114, conductors 113 must be adapted thereto, the arrangement of contacts 114 and conductors 113 may be simplified where there is the ability to define the respective patterns of contacts on electronic device 120 and on next-level substrate 140.

[ 060] Interposer 110 is then laminated to a semiconductor wafer or semiconductor device, i.e. interposer 110 is placed against such wafer or device with the plated ends 112a, 112b,... of conductive vias 112 against the contacts of such wafer or device and connected thereto by solder or conductive adhesive connections 124. If it is desired to provide additional strength to the mounting of the semiconductor wafer or device to interposer, or to protect the connections therebetween against moisture or other foreign matter, the space between interposer 110 and the semiconductor wafer or electronic device may be filled with an underfill adhesive. Type MEE7650-5 flexible thermosetting adhesive available from AI Technology is suitable for such underfill. The flexible thermosetting adhesives utilized for dielectric layer 111 and for conductive vias 112 are cured fully before the semiconductor wafer is separated into individual semiconductor devices. The preferred adhesives are cured at a suitable combination of temperature and time, typically for about 0.01 to 24 hours at a temperature between about 80°C and 250°C.

[ 061] FIGURES 7A, 7B and 7C are side cross-sectional diagrams illustrating the fabrication of an interposer 110 as described above in which flexible dielectric adhesive layer 111 is formed prior to conductive vias 112, and FIGURE 7D shows the interposer 110 so made attached to a semiconductor wafer 1120. FIGURE 7A shows a metal sheet or foil 113 that is provided with at least two relational alignment holes 119 that are utilized to align the various stencils or masks, or the various other layers with metal foil 113 during fabrication of a flexible adhesive interposer 110. Where flexible adhesive layer 111 is applied to metal foil 113 by stenciling or screen printing or the like, the masks, stencils and screens therefor each include a like set of relational alignment holes that are aligned with relational alignment holes 119 of metal foil 113, for example, by alignment pins passing therethrough. The masks, stencils and/or screens employed in the deposition of flexible adhesive to form flexible adhesive

layer 111 define via holes 117 therethrough. Where additional thickness of flexible dielectric adhesive layer 111 is desired than can be produced by a single deposition, a second deposition is made after drying or B-staging flexible adhesive layer 111-1 to form flexible adhesive layer 111-2 having the same pattern and via holes 117 as does layer 111-1. Further layers 111-n of flexible dielectric adhesive may be utilized to achieve the desired thickness.

[ 062]       Where flexible adhesive layer 111 (or layers 111-1, 111-2) is a thin sheet or membrane of dried, B-staged or partially-cured flexible dielectric adhesive that is laminated to metal foil 113, such thin sheet or membrane may have via holes 117 already formed therethrough, such as by drilling, punching, die cutting, laser cutting or the like, or via holes 117 may be formed after lamination, such as by laser cutting or laser drilling. Thin sheet 111 beneficially includes a set of relational alignment holes corresponding to those of metal foil 113 for alignment therewith, such as by alignment pins. An oxidation-resistant coating 113a is preferably provided on metal foil 113 where it is exposed at the bottoms of via holes 117.

[ 063]       Conductive vias 112 are formed in via holes 117 preferably by depositing flexible conductive adhesive onto the back side of metal foil 113 exposed through via holes 117 to substantially fill via holes 117, as illustrated in FIGURES 7B and 7C. Metal foil 113 is patterned, for example, by conventional photo-etching, to define conductors and contacts 113. A layer of solderable material, and preferably an oxidation-resistant layer, 112a - 112f and 114a - 114f is deposited onto flexible adhesive conductive vias 112 and conductors and contacts 113, either prior to or subsequent to the patterning of metal foil 113, but preferably subsequent thereto. Silver, gold, nickel, nickel-gold, nickel-palladium and other oxidation resistant metals, or copper, tin, lead, or indium, may be deposited, preferably by plating, so as to provide suitable solderability and/or bonding to electrically-conductive adhesives. Depending upon the pattern formed in metal foil 113, the electrically-conductive connections formed through flexible adhesive interposer 110 may be "straight-through" connections as illustrated in FIGURE 7B, or may provide "fan out" or redistribution of the contact pattern as illustrated in FIGURE 7C and as is convenient where the dimension and pitch of the contacts of electronic device 120 are too fine to

permit straight-through connection to conventional electronic substrates 140.

[ 064] Flexible adhesive interposer 110 so formed is shown attached to semiconductor wafer 1120 in FIGURE 7D, but prior to the patterning of metal layer 113. Connections 124, which may be solder or electrically conductive adhesive, join  
5 wafer-sized interposer 110 to semiconductor wafer 1120 with corresponding contacts 1124 of wafer 1120 electrically connected to the corresponding conductive vias 112 of interposer 110. Connections 124 may be solder connections or flexible conductive adhesive, as desired. Metal foil layer 113 is patterned to leave the desired pattern of solderable contacts, ones of which connect by conductive vias 112 and connections  
10 124 to the appropriate contacts 1124 of the individual electronic devices comprising semiconductor wafer 1120.

[ 065] The flexible adhesive interposers having solderable flexible conductive adhesive conductive vias according to the present arrangement may be utilized in a wide variety of applications for mounting and/or packaging of electronic devices such  
15 as semiconductor devices, integrated circuits, transistors, diodes, resistors, capacitors, inductors, and networks thereof. Such interposers may be utilized in packages for one or more electronic devices, for example, in the packages described in U.S. Patent No. 6,376,769, (Patent Application Serial Number 09/524,148) entitled "HIGH-DENSITY ELECTRONIC PACKAGE, AND METHOD FOR MAKING SAME" filed March  
20 14, 2000.

[ 066] FIGURE 8A is a plan view of an alternative embodiment of a flexible adhesive interposer 210 relating to the present arrangement and employing plural layers of flexible dielectric adhesive 211. A 6x6 array of contacts 212 on the "top" surface thereof (the surface visible in FIGURE 8A) are indicated by solid circles  
25 enclosing a number 1, 2 or 3 that indicates the number of layers of flexible dielectric adhesive 211 that the conductive via directly therebelow passes through on a "straight-through" basis. The 6x6 array of contacts 212 are to connect, for example, to the corresponding array of closely-spaced fine-pitch contacts on a 36-contact electronic device such as a semiconductor chip or other electronic component. A  
30 fanned-out array of contacts 214 on the bottom or opposing surface of flexible adhesive interposer 210 is indicated by dashed circles, each one connected to a



corresponding one of contacts 212 by an electrical conductor indicated by a dashed line 213. The array of contacts 214 are to connect, for example, to a next-level electronic substrate (not shown), such as a semiconductor wafer. By way of notation, lower-case letter suffixes a - f designate rows of contacts of the 6x6 array of contacts, and numerical suffixes indicate the number of layers of flexible adhesive above the item so designated. For example, conductor 213-1 is between the first and second adhesive layers 211-1 and 211-2, respectively. Contacts 212 and 214 typically represent the oxidation-resistant metal coating, such as nickel-gold or gold or nickel-palladium, platinum, on conductive vias 212.

10 [ 067] FIGURE 8B is a cross-sectional view of the flexible adhesive interposer of FIGURE 8A particularly showing the use of plural layers 211-1, 211-2, 211-3 of flexible dielectric material. The example conductive connection between contact 212a and 214a is provided by a conductive via 212-123 which passes straight through first, second and third flexible adhesive layers 212-1, 212-2, 211-3, respectively. The example conductive connection between contact 212b and 214b is provided by a conductive via 212-12 which passes straight through first and second flexible adhesive layers 212-1, 212-2, by a conductor 213-2 located at the interface between the second and third flexible adhesive layers 211-2 and 211-3, and by a conductive via 212-3 which passes straight through third flexible adhesive layer 211-3. The example conductive connection between contact 212f and 214f is provided by a conductive via 212-1 which passes straight through first flexible adhesive layer 212-1, by a conductor 213-1 located at the interface between the first and second flexible adhesive layers 211-1 and 211-2, and by a conductive via 212-23 which passes straight through second and third flexible adhesive layers 211-2 and 211-3.

25 [ 068] In the embodiment of FIGURES 8A and 8B, conductive vias 212 and conductors 213 are flexible electrically-conductive adhesive that is suitable to be plated, such as one of types ESP8350, ESP8450, ESS8450, ESP8550, and ESS8459 flexible conductive thermosetting adhesives, and ESP8680 rigid adhesive, all available from AI Technology, plated with a solderable metal such as copper, nickel, tin, silver, gold, palladium, platinum, nickel-gold, nickel-palladium and the like, and/or a combination and/or alloy thereof. Flexible dielectric adhesive layers 211-1,

30

211-2, 211-3 are of flexible dielectric adhesives as described in relation to flexible adhesive interposers above.

[ 069] In a typical fabrication sequence, flexible dielectric adhesive layer 211-1 is deposited with via holes therein on a metal layer or is laminated thereto. Via  
5 conductors 212-1 are flexible conductive adhesive deposited into the via holes through flexible adhesive layer 211-1. Conductors 213-1 are flexible conductive adhesive deposited on flexible adhesive layer 211-1, and are dried or B-staged. Flexible dielectric adhesive layer 211-2 is printed thereon with via holes therein, or may be laminated thereto. Via conductors 212-2 are flexible conductive adhesive  
10 deposited into the via holes through flexible adhesive layer 211-2. Flexible conductive adhesive conductors 213-2 are deposited on flexible adhesive layer 211-2 and are dried or B-staged. Flexible dielectric adhesive layer 211-3 is printed thereon with via holes therein, or may be laminated thereto. Via conductors 212-3 are flexible conductive adhesive deposited into the via holes in flexible adhesive layer 211-3. The  
15 metal layer may be patterned at any convenient point in the foregoing process. Contacts 212a-212f and 214a 214f are plated of a solderable, and preferably oxidation resistant, metal as described above. To the extent via conductors 212 pass straight through one or more layers, they may be deposited through one or more layers at a time, as may be convenient. It is noted that plural-layered flexible adhesive  
20 interposers similar to interposer 210 may include greater or lesser numbers of layers 211-1, 211-2 and so forth, of flexible adhesive and may include other arrangements and/or patterns of contacts 212a, 212b ... 214a, 214b..., conductive vias 212 and conductors 213 as may be desirable or convenient in a particular application.

[ 070] In utilizing interposer 110, solder balls or bumps 124 and/or 134 are  
25 formed in conventional manner on the conductive vias 112 and/or the contact portion 114 of patterned conductors 113 for connecting to electronic device 120 and to a next-level substrate, including another electronic device or another similar interposer, as is described below.

[ 071] It is noted that alignment holes are also useful, either alone or in  
30 conjunction with visual fiducial marks, in positioning and aligning a flexible interposer 110, or a panel or strip of flexible interposers 110, for placement of

electronic components 120 thereon using automated component placement apparatus, such as conventional surface mount technology (SMT) pick-and-place equipment, flip-chip bonders, and the like.

[ 072]           Also preferably, a plurality of flexible interposers 110 are formed as a panel or strip of interposers 110 for efficiently processing plural interposers 110, for example, for screening, stenciling, or laminating of the flexible adhesive layers 111 and the metal foil 113, for patterning of the metal foil 113, for depositing conductive vias 112, and for plating of the solderable and/or oxidation resistant layer and possibly for the application of soldering flux. After plural flexible interposers 110 are formed in a panel or a strip, individual flexible interposers are cut or excised from the panel or strip for use. The thickness of each flexible adhesive layer 111 of flexible interposer 110 is preferably comparable to the height of the solder balls 124, 134 to be formed, i.e. typically in the range of about 75-200  $\mu\text{m}$  (about 3-8 mils), and more typically about 100-125  $\mu\text{m}$  (about 4-5 mils).

[ 073]           Referring again to FIGURES 7A - 7D, flexible dielectric layer 111 may be minimized or even eliminated as follows. Instead of depositing dielectric layer 111 as shown in FIGURE 7A, flexible conductive adhesive bumps 112 are deposited onto metal foil 113 and the metal foil 113 is laminated to or attached to semiconductor wafer 1120 with each of the conductive bumps 112 in contact with the corresponding contact 1124, producing an assembly as in FIGURE 7D with connections 124 provided by the flexible conductive adhesive vias 112, i.e. without separate connections 124. Metal foil 113 is then either patterned to leave metal contacts on each of conductive vias 112 or is etched away to leave the ends of conductive vias 112 exposed. The ends of conductive vias 112 are then covered with a solderable material, such as copper, nickel, tin, lead, or indium, and preferably silver, gold, palladium, platinum, nickel-gold, nickel-palladium or the like, such as by plating such material thereon, producing the structure shown in FIGURE 9.

[ 074]           Alternatively, the interposer arrangement of FIGURE 9 may be made directly on semiconductor wafer 1120 or an individual electronic device or an appropriate next-level substrate or a panel thereof. Wafer 1120 has a pattern of contacts 1124 thereon that are preferably plated with an oxidation-resistant material,

such as one of the precious metals, e.g., nickel-gold or gold, described above.

Typically, contacts 1124 are aluminum or copper pads of about 50 - 100  $\mu\text{m}$  (about 2 - 4 mils) diameter. A pattern of conductive flexible adhesive bumps 112 are deposited onto contacts 1124, preferably of a flexible conductive adhesive of the types described

5 above. Bumps 112 are typically of like diameter to the contacts onto which they are deposited, such as by screening, stenciling, dispensing, ink-jet printing or other suitable method, and have a height of about 25 - 250  $\mu\text{m}$  (about 1 - 10 mils). After conductive bumps 112 are at least dried or B-staged, and preferably are cured, a

solderable coating 114 is applied to the tops (ends) thereof to provide a solderable

10 contact. Suitable solderable coatings include copper, nickel, tin, lead, or indium, and preferably silver, gold, palladium, platinum, nickel-gold, nickel-palladium, and combinations and alloys thereof, applied such as by an electroless plating process

(preferred), or another suitable plating or flash coating process. A wafer 1120 and the individual electronic devices produced when such wafer 1120 is singulated, may then

15 be directly attached to a printed circuit board or other substrate by soldering. Such soldering may utilize conventional C<sup>4</sup> solder bumps, eutectic solder bumps, deposited either onto solderable contacts 114 of flexible interposer conductive vias 112 or on the corresponding contacts on a printed, circuit board or other next-level substrate.

Optionally, a dielectric adhesive layer may be deposited onto wafer 1120 around

20 conductive bumps 112 thereon for protecting wafer 1120 or for providing additional strength. The flexible dielectric adhesives types described above, such as types ESP7450, ESP7550 and ESP7675, are suitable for such optional dielectric layer.

[ 075] FIGURES 10, 11 and 12 are side cross-sectional schematic diagrams illustrating stages in the fabrication and application of another alternate embodiment

25 of a flexible interposer 110 according to the invention. In FIGURE 10, flexible adhesive dielectric layer 111 is deposited in paste form onto metal foil 113 or is laminated in sheet form thereto. Layer 111 includes a pattern of "blind" via holes 117, which are formed in the deposition or thereafter (as by photo-etching or laser drilling or the like or are present in the sheet adhesive as laminated, as described

30 above, to expose the otherwise covered surface of metal foil 113. The exposed portion of metal foil 113 at the bottom of via holes 117 is preferably coated with as

oxidation resistant material 113a, e.g., nickel-gold or the like, as described above.

The mask or stencil utilized in depositing adhesive layer 111 on metal foil 113, or the sheet of adhesive 111 laminated to metal foil 113, may be accurately positioned and aligned using two or more alignment holes 119 or similar fiducial indicia.

5     **[ 076]**         FIGURE 11 illustrates blind via holes 117 filled with conductive adhesive, preferably a flexible conductive adhesive as described above, to form conductive vias 112 therein, which vias 112 preferably extend above the surface level of dielectric layer 111. This layered structure is then laminated to a semiconductor wafer 1120 (or another electronic device or substrate or a panel of such items) with  
10     conductive vias 112 making connection to contacts 1124 of wafer 1120, either directly or by flexible conductive adhesive bumps or by coating conductive vias 112 with a solderable material, e.g., gold or nickel-gold or the like, as described above. Metal foil 113 is patterned, such as by photo-etching, either before or after the layered structure 110' is attached to semiconductor 1120, to leave solderable contacts 114.  
15     Contacts 114, which may be of the same, smaller or larger diameter than conductive vias 112, may be coated with a solderable material if needed for solderability, for example, with a solderable metal such as nickel-gold or the like as described above.

20     **[ 077]**         The resulting solderable flexible adhesive interposer 110, illustrated in FIGURE 12, is typically 25 - 250  $\mu\text{m}$  (about 1 - 10 mils) thick, and more usually 75 - 125  $\mu\text{m}$  (about 3 - 5 mils) thick. It is noted that the etching process limits the ratio of the diameter of contacts 114 to the thickness thereof to about two. A wide "ring" 118 of metal foil 113 may be left near the periphery of interposer 110 to provide additional mechanical strength and support, particularly in the locations of alignment holes 119 or other fiducial indicia. Ring 118 may be the same thickness as metal foil 113, as  
25     above, or may be slightly thinner, e.g., 50 - 100  $\mu\text{m}$  (about 2 - 4 mils).

30     **[ 078]**         FIGURES 11A and 11B are side cross-sectional schematic diagrams illustrating fabrication steps additional to the stage of FIGURE 11 for producing an alternate embodiment 210 of interposer 110 that has a substantially longer conductors 1112 for connecting between an electronic device and another substrate. Columns 212 of conductive metal, such as copper, aluminum, nickel, tin, lead, indium, gold or other suitable metal, are formed, such as by plating, on flexible conductive adhesive

vias 112 to increase the length thereof. Preferably, copper is electrolytically plated. Conductive vias 112 are preferably coated with a metal plating 112a, such as a gold, palladium, platinum, gold-nickel or gold-palladium layer, prior to the plating of the column 212 of copper or aluminum thereon to provide a more stable contact resistance therebetween. Metal columns 212 are preferably plated with a solderable metal 212a, which may also be oxidation resistant, such as a gold, palladium, platinum, gold-nickel or gold-palladium layer as above.

[ 079]            Optionally, as illustrated in FIGURE 11B, an additional layer 211 of flexible dielectric adhesive may be applied over flexible dielectric layer 111 and surrounding metal columns 212 where additional strength is desired for interposer 210. Preferably, both of layers 111, 211 are of the same type of flexible dielectric adhesive such as the adhesives identified above. It is noted that any number of layers of flexible dielectric adhesive may be deposited, each preferably being dried, B-staged or cured prior to the deposition of the next layer thereof, thereby to obtain any desired thickness of flexible adhesive. Metal foil 113 is patterned to define contacts 114 and optional peripheral strengthening ring 118, and contacts 114 may be plated with a solderable metal 114a, which may also be oxidation resistant, all as described above. Optionally, flexible dielectric adhesive 115, preferably of like type to that of layer 111, may be deposited in the space between the remaining portions of metal foil 113, i.e. surrounding contacts 114, 114a, where additional mechanical strength is desired.

[ 080]            Advantages of solderable flexible adhesive interposer 210 include that the increased length of conductors 1112, which length can exceed one or two times its diameter, provides additional flexibility in the connections between an electronic device and the substrate to which it connects, thereby increasing the reliability of such connections under thermal cycling stress, even if both ends of conductors 1112 are soldered. Moreover, because each of conductors 1112 contains a portion provided by conductive via 112 that is flexible because it is of a flexible conductive adhesive, conductor 1112 is itself flexible and also serves to reduce the stress produced by thermal cycling conditions. In addition to use for connecting an electronic device to a substrate, flexible adhesive interposers 110, 210 may be applied to an electronic and utilized for making connections thereto for the purpose of testing such device,

including semiconductor devices on a semiconductor wafer or as individual devices singulated from such wafer.

[ 081] It is noted that where plural-layered solderable metal coatings are employed, such as the nickel-gold or nickel-palladium coatings, the nickel is plated onto the copper or aluminum metal and the gold or palladium is plated onto the nickel layer so as to be exposed for coming into contact with the solder or conductive adhesive that will be placed in contact therewith.

[ 082] Layers of flexible adhesive are typically deposited at a wet thickness of about 150-300  $\mu\text{m}$  (about 6-12 mils) and more typically of about 225  $\mu\text{m}$  (typically about 9 mils), which dries and/or cures to a thickness of about 150  $\mu\text{m}$  (about 6 mils). Via openings 117 typically range between about 25 $\mu\text{m}$  to 2.5 mm (about 1-100 mils) in diameter, with an about 300- $\mu\text{m}$  (about 12-mil) diameter being typical for some via openings and an about 250- $\mu\text{m}$  (about 10-mil) diameter being typical for slightly smaller via openings 542, and about 100  $\mu\text{m}$  (about 4 mils) being typical for semiconductor contacts. Where the metal foil is laminated to a sheet of flexible adhesive, lamination is at a temperature typically between 80 °C and 150 °C with lamination heating and pressure applied by heated rollers.

[ 083] The methods herein are suitable for making solderable flexible adhesive interposers individually or for making a number of interposers contemporaneously, as where panels or webs of metal foil and/or of flexible adhesive layers are utilized in a batch process or in a continuous process. In a batch process, a panel or panels, e.g., a 25 by 31 cm (about 10 by 12 inch) panel or a 31 by 50 cm (about 12 by 20 inch) panel, of the aforementioned material or materials is utilized and a number of interposers are formed therewith and thereon, such as by screen and/or stencil deposition of layers of flexible adhesive. In a continuous process, a web or strip, e.g., of a 12.5 to 25 cm (about 5 inch to 10 inch) width, is utilized and is moved along as the various layers are roll deposited thereon or are roll laminated thereto. The web or strip may have drive sprocket holes along one or both edges thereof for moving it along in a controlled manner. After a plurality of flexible adhesive interposers are formed in a panel or strip, the panel or strip, as the case may be, is excised to produce the individual interposers therefrom.

[ 084]           If either the flexible dielectric adhesive or the flexible electrically conductive adhesive or both is a thermosetting adhesive, it is preferred to cure such thermosetting flexible adhesive prior to forming a solderable electrically conductive metal layer thereon and prior to etching or otherwise patterning the metal foil layer. It is noted that an adhesive, whether dielectric or conductive, can be said to withstand soldering temperature if it is a thermosetting adhesive that does not melt or substantially change in its electrical and mechanical properties when heated to the melting temperature of solder or is a thermoplastic adhesive having a melt flow temperature that exceeds the melting temperature of solder.

[ 085]           While the present invention has been described in terms of the foregoing example embodiments, variations within the scope and spirit of the present invention as defined by the claims following will be apparent to those skilled in the art. For example, while the electronic device contained within each of the various embodiments of the package described herein are described as a semiconductor chip or die, such as an integrated circuit or the like, such devices may include other types and kinds of electronic components such as resistors, capacitors, inductors, and networks of such devices and combinations thereof, as well as plural semiconductor chips or die, either alone or in combination with other components.

[ 086]           Where plural layers are employed in the flexible dielectric adhesive interposers described herein, it is evident that a greater or lesser number of layers may be utilized to achieve more complex or simpler fan-out patterns as may be convenient in any particular instance, without departing from the inventive concept described herein or the method for making a particular embodiment or alternative thereto.

[ 087]           Flexible adhesive interposers according to the present invention may be provided with bumps of solder or of conductive adhesive on the contacts thereof to facilitate the attachment of semiconductor chips and other electronic devices thereto, and/or with a pre-applied epoxy underfill adhesive, such as AI Technology type ESP7675, thereon, and/or with a pre-applied adhesive film, such as AI Technology type ESP7450, thereon for bonding other items, such as a shaping frame or cover, thereto.

[ 088]           In addition, the electronic device packages of the present invention



may be employed in combination with other conventional mounting technology, such as ball-grid array (BGA) technology and pin-grid array (PGA) technology. In such case a package according to the present invention is mounted to a conventional BGA or PGA solderable substrate which is in turn attached to a next-level substrate in conventional BGA or PGA manner.

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